TATUNG

C Series Colour Television

SERVICE INFORMATION

Systems I, B,G, D,K

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C SERIES SERVICE MANUAL

1. SAFETY AND ISOLATION

Under no circumstances should any form of repair or maintenance be attempted by any person other than a competent technician or engineer. Most of the circuitry on the chassis is isolated from the mains by T801,C811,C827,R815 and R816 and 6mm air gaps. To maintain this safety factor ensure that, after repair, any gaps or leakage paths are not reduced by protruding wires, etc., following component replacement.

NOTE: although the output supply paths from the power supply section are isolated from the incoming mains supply, the bridge rectifier and the control and regulation circuits are not isolated. Therefore, when servicing the power supply section of the chassis, the mains input should be connected via an isolating transformer of at least 200 watts rating.

The power supply section remains charged with respect to chassis for 30-60 seconds after switching off. Care should be taken to avoid touching the power supply area of the chassis during this time.

Components marked ! on the parts list are safety approved types and should be replaced only with components supplied or approved by our Service Department. It is also recommended that components not marked with the safety symbol should be replaced with parts of the type originally fitted. This applies particularly to those resistors which are stood off the printed circuit boards.

1.1 Handling Precautions - Static Electrical Charges

The receiver contains devices which may be damaged by static electrical charges during handling. To avoid damage, soldering irons should be earthed, and service personnel should wear wrist straps earthed via a 1M ohm resistor. If the latter is not practical, they should discharge themselves by touching an earthed point. Sensitive static devices should be packed in suitable conductive containers.

IMPORTANT: although the receiver chassis is isolated, the mains supply should be disconnected during service replacement of such static devices.

2. SWITCHED MODE POWER SUPPLY

The self-oscillating switching converter circuit centres around IC801 (TDA4605) which provides all the necessary control and protection functions. The operating frequency varies in the range 20-80kHz dependent upon the load conditions. IC801 controls the MOS power transistor (Q801) which switches T801 primary winding across the rectified mains voltage stored in the reservoir capacitor (C808). AC output voltages of 9.5V, 18V and 115V, developed at taps on the secondary winding, are rectified and smoothed by separate diode/capacitor networks.

The Q801 drive from pin 5 of IC801 maintains constant secondary winding voltages regardless of input or load changes. A control voltage, derived from a secondary winding, is rectified/smoothed by D808/CE806. The attenuated control voltage is applied to IC801 pin 1 and is used to match pin 5 output pulse frequency to secondary load conditions. RV806 (SET HT) adjusts the proportion of the control voltage fed to pin 1 of IC801 and thereby adjusts the output voltage. R811 and C807 provide pin 2 of IC801 with a voltage proportional to Q801 drain current. This is used in the IC to control the pulse duty factor at pin 5. The AC control voltage from T801 secondary is attenuated by R805 and fed to pin 8 of IC801 to ensure correctly timed drive pulses for Q801. The zero passage detector at pin 8 senses a zero crossing and thereby enables the control logic. The supply to pin 6 of IC801 is developed by D807 and C803 from the secondary winding of T801. Start-up voltage is provided via R802 and R803 from a "half-wave" point on the mains rectifier bridge.

IMPORTANT: Pin 4 is approximately -330V relative to the chassis.

2.1 Voltage Adjustment

With the receiver locked to a normal picture signal, reduce the brightness, contrast and A1 controls to minimum *i.e.* zero beam current. Connect a suitable voltmeter across C407 and adjust RV806 for a reading of 115V (14" and 20" standard tube models), or 109.5V (15" and 21" FST tube models).

2.2 Secondary circuits

The secondary windings of T801 are half-wave rectified to provide the various supply rails required for the chassis.

The +12V rail is regulated by IC803, and associated components. TR802 is controlled by the microprocessor (IC701) to disable the +12V supply when standby mode is selected. The +9V supply is derived from the +12V supply rail by IC802 and ZD806, the +9V supply is used to power the I.F. daughter board and parts of the video-chroma-deflection circuit (IC543). The +5V supply is derived from a dedicated winding of the transformer T801 by IC804, and is used to power the microprocessor (IC701) and the infra-red receiver (IC750).

2.3 HT supply (109.5V/115V)

Regulation of the HT rail is provided by the action of the power-supply control device (IC801). The HT supply is set for optimum by adjustment of RV806, the remaining secondary voltages will alter in sympathy with the HT supply and therefore have IC regulators to ensure that the correct low voltage supplies are provided independant of the HT setting.

3. TUNER AND I.F. STAGES

3.1 Tuner

The main chassis is fitted with a UHF (System I) or UHF/VHF (Systems B/G/D/K) tuner, TU001. Tuning is achieved by varying the d.c. control voltage at pin 7, TU001. The microprocessor daughter board selects the appropriate tuning voltage in response to the local or remote controls. A stable +33V tuning voltage supply is provided by a temperature

compensated regulator, IC001, which is driven from the HT supply.
In this receiver the AFC is sampled by the microprocessor and frequency correction is achieved by (microprocessor) adjustment of the tuning voltage. There is no direct connection of the AFC output from the I.F. to the tuner.

For most aerial input signal levels the tuner operates at full gain. At high signal levels the gain of the tuner is reduced by an AGC voltage generated in the I.F. stage. The AGC output from the I.F. panel (pin 5 PL101) is applied to the tuner (TU001) via pin 1.

3.2 AGC adjustment

Correctly tune the receiver to a 10mV R.F. modulated carrier at approximately channel E 58 (767.25MHz). Monitor the tuner output (pin 9 PL101) with an oscilloscope and probe calibrated to read accurately at 40MHz. Adjust RV101 to obtain the following level at the peak to peak sync excursions:-

UK models	1.2V
German models	325mV
Other models	600mV

3.3 I.F. for System I Receivers

This is contained on the daughter board next to the tuner. The signal is fed from the tuner through the SAW Filter FL101, which filters unwanted frequencies, before being amplified by IC101. This ic also contains the vision and sound demodulators, L103 is the AFC coil and should be adjusted to give 2.5V at pin 12 PL101 when 39.5MHz is injected into the SAW Filter. L104 is the vision detector coil and should be adjusted to display a square corner, without overshoot or excessive 'rounding', at the beginning of the peak white section of a colour bars signal at the emitter of TR101. The sound demodulation uses a Ceramic discriminator (FL103) and a Ceramic filter (FL102) and is therefore adjustment free. The video output from pin 15 of IC101 is filtered by L108 and R104, FL104 is a 6MHz trap to remove the sound carrier from the video which is then buffered by TR101 and fed to the main chassis.

3.4 I.F. for System B/G/D/K Receivers

This daughter board contains one dual output SAW Filter or two separate filters for the vision and sound I.F.'s depending on the receiver type. IC101 contains the I.F. amplifiers and demodulators for the separate sound and vision channels. The vision I.F. uses L107 for AFC and should be adjusted to give 2.5V dc at pin 3 PL101 when 38.9 MHz is injected into the SAW filter. L106 is the vision detector coil and should be adjusted to display a square corner, without overshoot or excessive 'rounding', at the beginning of the peak white section of a colour bars signal at the emitter of TR101. The composite video from pin 2 IC101 is filtered by L108 and R117, FL106 and R113 form a 5.5 MHz sound filter when fitted, before being buffered by TR101 and fed to the main chassis via PL101 pin 11.

The audio I.F. has its own detector coil L105 which should be adjusted until a null point is found where the video information at pin 21 IC101 is at minimum, the signal at pin 21 is then fed through two pairs of ceramic filters (FL102 & FL104 for 5.5MHz and FL103 & FL105 for 6.5MHz) to pin 19. The sound is then demodulated by IC101 using the detector coils L103 and L104. These should be adjusted for minimum distortion at pin 11 when the receiver is fed with a signal containing a 5.5MHz sound carrier frequency modulated with 1kHz for adjusting L103 or a 6.5MHz sound carrier frequency modulated with 1kHz for adjusting L104.

4. SYNC PROCESSING AND TIMEBASE GENERATORS

In addition to providing the luma/chroma decoding, IC543 provides deflection processing for the line and field timebase circuits. Using the composite video signal from the I.F. stage, the timebase section of IC543 produces line drive pulses (at pin 39) to switch the line drive transistors TR401 and TR402, and a field ramp voltage (at pin 29) to drive the field output circuit (IC301).

4.1 Sync Separator

The sync. seperator (pin 33, IC543) is fed with the composite video signal from the I.F. output (pin 11, PL101). The slice level for the sync seperator is set by the ratio of R542 and R543. The output from the sync. seperator is fed to a PLL circuit to correct the line oscillator frequency.

4.2 Line Timebase

Line sync. pulses are compared with the sawtooth waveform obtained by integrating the line flyback pulse. The line time constant is set by R540, C524, and C525 via pin 36, IC543. For VCR use (when a programme number ending in '9' is selected) TR503 is turned 'off' and modifies the time constant by switching out R539 and C505. The line oscillator output is fed to an internal driver transistor which produces a line drive waveform at pin 39, IC543. The line oscillator frequency is determined by a ceramic resonator running at 32x line frequency (503kHz), there is therefore no line oscillator frequency adjustment on this receiver.

4.3 Field Timebase

The output pulses from the internal sync. seperator (IC543) are fed via a built-in integrator network, the output of this network resets the countdown circuit which drives a ramp voltage appearing at pin 29, IC543. The ramp starting voltage and timing is determined by the network attached to pin 31, IC543. The sawtooth output is compared with a feedback voltage from the vertical scan coils via R302 and R304 into pin 32, IC543. The comparator generates a ramp voltage (at pin 29,IC543) which is used to drive the field scan integrated circuit IC301.

4.4 Timebase Adjustments

The line oscillator (free-running) frequency is determined by a 503kHz ceramic resonator XL501. There is no line frequency adjustment in this receiver.

Adjust L402 and RV535 for correct picture width and centring.
Adjust RV547 and RV312 for correct screen height and centring.

5. LINE SCAN AND EHT

Pulses at line frequency from the sync. processor (see section 4) are fed to the base of TR401 which with TR402 in Darlington configuration forms the line driver. The line-drive transformer (T401) secondary provides a low-impedance pulse source to switch the line output transistor TR403. The line scan output circuit is a conventional energy recovery type with the deflection coils tuned during flyback by C404. 'S' correction is provided by C405.

A 26V supply for the field timebase is taken from a secondary winding on the diode-split transformer (T402). This is rectified by D403 and smoothed by CE409.

A further secondary winding provides power for the picture tube heaters and a reference flyback pulse for the sync. processing part of the video-chroma-deflection processor (IC543). Output from a tap on the primary winding, rectified by D402 and smoothed by CE408, provides a 200V supply for the video output amplifiers on the tube-base panel.

The EHT supply to the picture tube (24kV nominal) is produced within the diode-split transformer (T402) by a 3-stage diode split overwind. The leakag inductance of T402 and the distributed capacitance of it's overwind are tuned to harmonics of the line flyback frequency to ensure good EHT regulation. An integral thick-film resistor network is connected across the first section of the overwind to provide adjustable focus and A1 voltages for the picture tube.

6. FIELD SCAN

Field scan is carried out by IC301 using a 26V supply derived from the line scan output circuit. The field drive ramp present on pin 29 of IC543 is fed via R550 to pins 1 and 3 of IC301. The scan current output at pin 5 of IC301 is fed to the field scan coils. The current in the coils is sampled by R307 with the resulting voltage fed back to pin 32 of IC543. The gain of the field scan amplifier is controlled by R302,R305 and R307. High frequency stability is maintained by C302 and R303.

For rapid flyback, IC301 is equipped with a flyback generator. The 26V supply to IC301 during scan is applied to pin 6 via D301. During flyback the voltage is transferred through C306 to pin 8 causing the voltage to double. This results in a more rapid collapse of the scan coil field until the voltage across the coils falls below 26V when pin 8 swings back to low voltage and the cycle is repeated.

7. VIDEO DECODING

The luma signal processing and colour decoding are also implemented by IC543. The luminance and chrominance signals are first separated by FL502; this also incorporates a delay line to compensate for the difference between the luma and chroma processing times. The luminance signal is then fed through RV505 into pin 58, IC543. RV505 sets the tubebase video drive level and should be adjusted to give 400mV black to white level at pin 58, IC543.

The chrominance signal is attenuated and fed into pin 20 IC543. It is then split and fed directly to the internal decoding circuits and from pin 14 it is fed to the delay line via RV560, to adjust the amplitude of the delayed signal, and L508, which adjusts the phase of the delayed signal. This delayed signal is returned to pin 12 to be combined with the direct signal. The demodulated colour signals present at pins 2 and 64 are filtered and attenuated by R565, R566, C558, C560 for the R-Y and R501, R502, C501, C507 for the B-Y.

7.1 Picture Controls

Analogue picture control (colour, contrast and brightness) is provided by the microprocessor panel these are then fed directly to the decoder. The controls have the following ranges set by resistors on the microprocessor panel:-

Control	Min	Normalized	Max	Pin no.	
Brightness	2.9	3.3	3.8	48	
Saturation	2.9	3.3	3.8	7	
Contrast	2.9	3.3	3.8	59	(varies with screen size)

The contrast control is also used to control the beam limit. When the beam current approaches 0.8mA the voltage across R409 falls to below the voltage at pin 59 IC543 and current flows through R410, R514 and D502 reducing the contrast voltage and limiting the drive to the tube.

7.2 On Screen Display

The on screen display is achieved by applying signals from the microprocessor to the external Red and Green inputs of IC543 (pins 47 and 49), the OSD is enabled by applying 1.2V to pin 53 IC543.

7.3 Secam models

These adjustments can only be performed during Secam transmissions.
On models designed to receive Pal and Secam colour transmissions extra components are fitted. These are indicated on the circuit diagram by an S and comprise:-
L502 SECAM Ident coil: adjusted for maximum voltage at pin 23 IC543.
L503 Bell filter: adjusted for minimum overshoot on R-Y and B-Y signals at pins 60 and 62 of IC543.
L510 and L511 (R-Y and B-Y demodulators): adjusted for equal levels during blanking and black parts of signal at pins 1 and 63 respectively, see waveform diagrams.
L509 and C509 form an extra trap which is switched in by TR505 and TR502, and their associated components, when SECAM is being received to reduce interference from the chroma signal appearing on the luma signal.

8. PICTURE TUBE BASE PANEL

The picture tube-base panel includes the supplies to the tube electrodes with their associated components for circuit protection. Internal spark gaps are fitted in the tube socket for connection to the tube external dag coating. Also included on the panel are the video amplifiers TR201,TR202, and TR203, and their preset adjustments. The focus and A1 supplies are embodied in the diode-split transformer (T402).

To adjust the red, green and blue backgrounds; reduce the A1 control to minimum. Adjust the user brightness and contrast controls to their normalized settings and set the colour saturation control to minimum. Adjust each of the background controls R202,R203 and R204 so that the black level measured at each tube cathode (R904, R905, and R906) is 150V.

Increase the A1 control for correct overall black level on the display. Grey-scale corrections may now be carried out with only two of the background preset controls.

9. REMOTE CONTROL

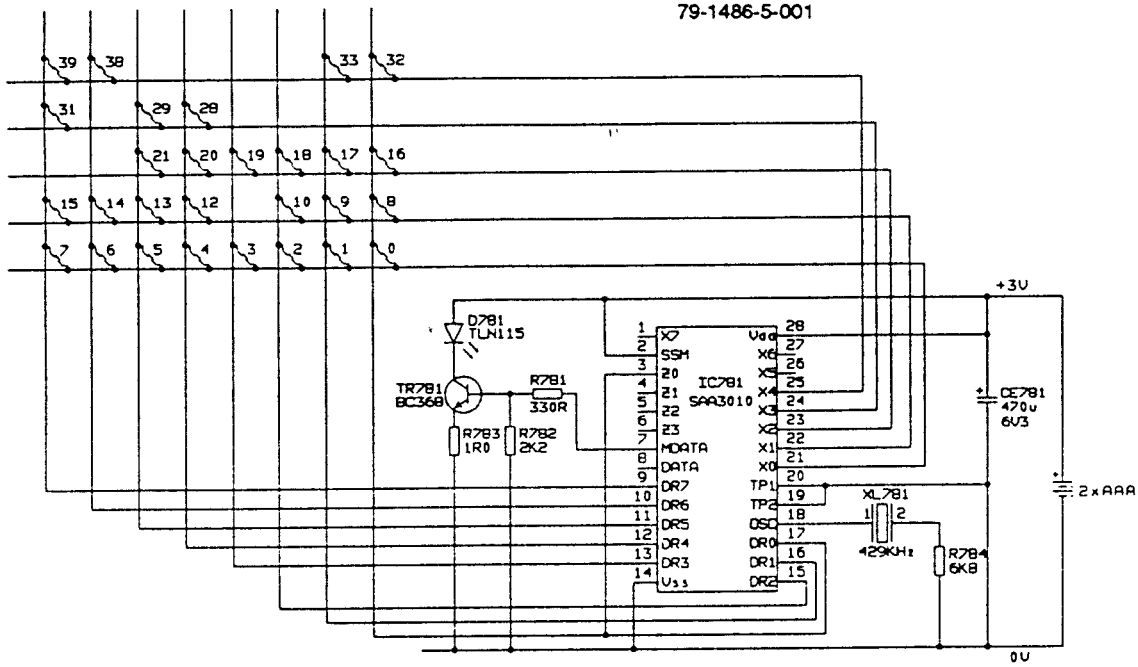
9.1 Infra-red transmitter

The infra-red transmitter consists of a single IC (IC781) which contains all the circuitry required to scan the rubber membrane keyboard and produce a series of pulses to drive the infra-red transmitting diode (D781). In the rest state, with no keys depressed, the drive lines (pins 9-13, and 15-17, IC781) are held in the 'low' state and the sense lines (pins 21-25, IC781) are held in a 'high' state by internal pull-up devices. If a key on the matrix is closed the key position is detected and the corresponding command code is produced at the transmitter output (pin 7, IC781). The command generated by IC781 is transmitted as a bi-phase code. The code consists of; 2 start bits, one control bit, 5 system address bits and the 6 command bits. The phase change during each bit period determines the value of the bit *i.e* a '0' or a '1' as shown in Fig. 9.4. The bi-phase code is modulated onto a 35.75kHz carrier frequency.

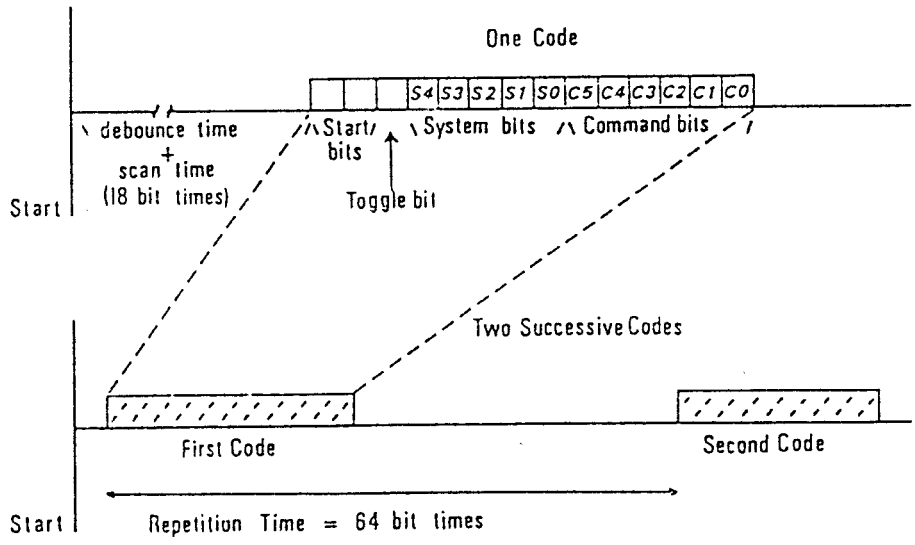
9.2 Infra-red receiver

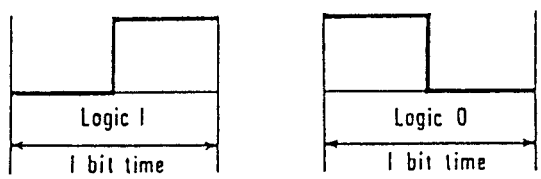
Reception of infra-red transmissions from the remote hand unit is performed by IC750. This IC is mounted close to the front of the main chassis. The coded infra-red signals are detected within the photo module IC750. IC750 incorporates the pre-amplifier and pulse stretcher which directly drive the microprocessor (IC701,pin 3). The pulse-stretched output, pin 3, is normally 'high' (>4.9V) and goes 'low' when an infra-red pulse is received. From IC750 the demodulated infra-red signal is taken via SK701 pin 1 to IC701 pin 3. Pointing a hand unit at IC750 and pressing any key should produce a series of highs and lows at IC701 pin 3 corresponding to the RC5 standard code for the remote key operated.

9.3 RC300 HAND UNIT CIRCUIT DIAGRAM - C Series



9.4 SAA3010 RC-5 TRANSMISSION





$3 \times 2^6 \times t_{osc} = 1{\cdot}79\,mS\ (typ)$

10. MICROPROCESSOR CONTROL SYSTEM

The microprocessor sub-panel holds two integrated circuits; the microprocessor MN15151GBC (IC701), and the non-volatile memory X2402P or equivalent (IC702). Situated around the microprocessor (IC701) are various circuits which provide interfacing with the rest of the 'C' chassis hardware. The (transmission standard) options available on the 'C' series chassis are selected according to the voltage applied to pin 21 of the microprocessor (IC701). For single standard (System I) receivers the voltage at pin 21 must be 2.5V ±0.2V, for multi-standard (System B/G/D/K receivers) the voltage at pin 21 must be less than 0.5V. On the main circuit board are two resistor positions R750 and R752 which provide the correct voltage to pin 21 of IC701 for the receiver system required.

C703 ensures that the microprocessor is reset at power up. For correct reset the voltage at IC701 pin 7 must remain at a logic '0' for a minimum of 50ms after the +5V rail has risen above +4.5V. Then the voltage at IC701 pin 7 should rise to a logic '1'. In any case, the voltage at IC701 pin 7 must be at a logic '1' 300ms after the +5V rail reaches +4.5V.

After the power supply, next most important to the functioning of IC701, and thus the whole receiver, is the clock crystal XL701. This component, in conjunction with C705 and C710 provides internal timing for the microprocessor and also the On Screen Display function. It should oscillate at 6MHz±5kHz as measured at the oscillator output (pin 44 of IC701), with an amplitude of 4.8V peak-peak.

The microprocessor requires inputs of vertical and horizontal sync signals for two reasons. Firstly, they provide references for the internal OSD circuits. Secondly, the processor uses the vertical sync waveform to decide if a valid TV signal is present. Vertical sync signals should be present at IC701 pins 22 and 36. They should be negative going with a high level amplitude of +5V and low level of 0V. The pulse widths for the vertical syncs should be 80us±10us. The horizontal sync signal at IC701 pin 32 should again be negative going, with the high level amplitude being +5V, the low level 0V. The pulse widths for the horizontal syncs should be 12.7us±1us.

Normally the mains switch momentary contact input (IC701 pin 18) rests at +5V. However, when the mains switch is closed, charge (and thus voltage) is transferred from CE830 via the momentary contact, SK702 pin 2 and R704 to CE704. The momentary contact by its nature is closed for only a very short time, so CE704 is soon isolated electrically from CE830. The potential now on CE704 causes a small current to flow through R729 and the base-emitter junction of TR713. Monitoring IC701 pin 18 (collector of TR713), should show that the voltage there remains below 0.5V for between 2.5 and 3.0 seconds before rising to >=+4.5V after five seconds. By this means the microprocessor is able to determine at power-on whether or not the a.c. mains voltage was applied by operation of the mains switch.

On every remote or local key press, IC701 pin 5 changes from a logic '1' to a logic '0' for about 250ms. In turn this pulses TR706 on for the same length of time, so lighting the LED D750 at the front of the motherboard to confirm operation.

The microprocessor (IC701) has a 14 bit pulse-width modulated (PWM) tuning output (pin 17), which is supplemented on the 'C' series chassis by a 6 bit true analogue output (pin 37) for very fine manual tuning and AFC adjustment. The tuning output switches TR704 on and off, thus chopping the +33V supply through R713 into a rectangular waveform on TR704 collector. This waveform is smoothed by the network of R716/C709/R715/C708. IC701 pin 37 has a 0V to +5V swing, which is reduced to 0V to 88mV by the potential divider R734/R736. This 'fine-tuning' voltage is used to modify the main, PWM-derived tuning voltage via R735. The total possible change in the tuning voltage output at SK702 pin 18 is 0.0V to 31.0V. Further smoothing close to the tuner is provided by R004/C004.

For System I version (PAL-only) PAL is always forced by R705 and R706 and the microprocessor has no control over the standard.
The System B/G/D/K versions of the 'C' series have been designed to work in either PAL or SECAM colour standards. On each programme the receiver allows the user the option of forcing the TV into either PAL or SECAM, or letting the colour decoder (in IC543) select the appropriate standard automatically.
Pin 23 of IC701 switches between automatic and manual modes. In the high state TR711 is on, so the anode of D504 on the main board is grounded. This leaves pin 21 of IC543 free to find its own level, which is the automatic mode. With IC701 pin 23 low and TR711 off, IC543 pin 21 is held at +6V by the combination of R527, R528 and D504. This signals IC543 that the vision standard should be selected according to the voltage on pin 11.
Selection of PAL or SECAM is performed by pins 29 and 31 of the microprocessor. For PAL pin 31 goes high, turning on TR710 and TR707. Also pin 29 stops pulling low, so TR708 is turned on by R702. The voltage at the junction of R710 and R711, and thus at IC543 pin 11, is +6V.

For SECAM, IC701 pin 31 is set to the low state - TR710 and TR707 are off. TR708, however, is switched on, pulling IC543 pin 11 low.
In automatic standard selection both pins 29 and 31 of IC701 are low; IC543 pin 11 is free to find its own level.

Control of volume is provided in 64 steps by the pulse-width modulated (PWM) output on IC701 pin 16. The amplitude of the rectangular wave on pin 16 is not constant, but varies with the actual PWM value. R730 leads the volume DAC output to CE607 on the main board via SK702 pin 11. The DC voltage at SK702 pin 11 should cover the range 0.4V to 11.9V as the Volume control is adjusted from the lower end of the range to the upper end.

To prevent the 'C' series television being used with anything other than a normal broadcast or pre-recorded signal, the audio is muted when no vertical sync pulses can be detected. This feature is a legal requirement in certain countries. With a correctly tuned TV signal or test card applied to the tuner input socket, IC701 pin 10 should have a steady logic '0', as should SK702 pin 9 and the audio power amplifier IC601 pin 3 (mute input). Removing the signal, or indeed changing the field sync frequency by more than ±6%, will cause IC701 pin 10 to go to a logic '1' (>2.7V), and the audio output of IC601 will be muted.

The AFC output of the I.F. panel is brought onto the microprocessor board at SK702 pin 14, and then is routed to IC701 pin 19. Noise filtering is provided by C706. R703 is the lower half of a potential divider, the upper resistor being on the I.F. panel (R117 for system I, R110 for systems BG/DK). This signal has a range of approximately +0.5V to +4.5V. When a television signal is correctly tuned in, the voltage on IC701 pin 19 should be 2.5V ±300mV. However, the microprocessor will attempt to centre the AFC voltage on 2.5V even if, due to mis-alignment of the I.F. for instance, the TV signal is not then correctly tuned.

After channel change a test is made for the presence of vertical sync pulses. If the test result is positive it is certain that a TV station is fairly near by. High gain AFC is applied, followed by medium then low gain AFC. Any subsequent drift in the signal is tracked by the low gain AFC. If the signal disappears for any reason, the low gain AFC is defeated for the duration of the signal loss.

UK models of the 'C' series have the tuner +12V supply permanently wired and no band-switching takes place. System B/G/D/K Receivers incorporate band selection by switching +12V to the appropriate tuner band supply pin. The switching is performed by TR701 (UHF), TR702 (VHFIII), or TR703 (VHFI).

Provision has been made on the 'C' series receiver for switching to a shorter time constant, for use with irregular syncs from a video recorder, on all programme numbers ending in the figure '9'. Pin 24 of IC701 is taken low to turn off TR503 which otherwise short circuits the high-value resistor R515.

11. SYSTEM TEST MODE

The system test mode provides extra functions for the service engineer that are not available to the customer. All test functions are controlled using the remote-control hand-unit supplied, or the local control keys.

11.1 Entering Test Mode by Microprocessor Reset

To enter test mode, switch the set on by its mains switch, at the same time holding closed the Volume Down key. This combination of actions inform the microprocessor that system test mode is required. The microprocessor will remain in test mode until it receives the normalize command from the remote hand unit, or until it is reset again.
When in test mode the various service/factory tests and set-up functions of the microprocessor can be selected by local keys, and by using a normal 'C' series hand-unit (RC300).

11.2 Non-volatile memory Initialization

On a new microprocessor panel, or when the non-volatile memory chip IC702 has been replaced for any reason, the new i.c. must be initialized with defaults for certain tuning and other parameters. To do this it is first necessary to put the microprocessor (IC701) into its test mode, as described above.

11.2.1 Non-volatile memory (non-tuning) default parameters.

On entry to test mode (after the CRT has warmed up) a green 'normalize' symbol will be displayed to confirm that the non-volatile default parameters have been stored. If there is no OSD, try pressing the local Volume Down key again. This test writes the non-tuning defaults to non-volatile memory. The parameters affected are; Volume (set to 25% level), Brightness, Contrast, and Colour Saturation (all set to 'normalize' position - mid-point on bargraph display), and the maximum volume limit is removed.
During the test execution activity will be seen on the serial bus i.e. alternate logical '0's and '1's; IC701 pin 47 is clock & 48 is data. Completion of the test is signalled on the OSD by the normalize symbol.

NOTE: Following this test it may still be necessary to defeat the local control 'child lock' feature, depending upon what brand of non-volatile memory is installed. Switch the set on by its mains switch, while holding closed the Programme Up key (fourth key from left).

11.2.2 Non-volatile Memory default tuning parameters.

Executed on operating the local Volume Up key whilst in test mode, this test writes the tuning defaults to non-volatile memory. The parameters affected are given in the table below.

Prog	Channel (Nominal)	Frequency (MHz)(Nominal)
1	62	799.25
2	31	551.25
3	37	599.25
4	21	471.25
5	68	847.25
6	02(E2)	48.25
70	9(E9)	203.25
8	58	767.25

Also the last programme stored is set to programme 1.

NOTE: in a Voltage Synthesis system the microprocessor cannot itself determine exactly the correct tuning voltage required to tune a particular signal. For this reason the default tuning values are calculated to set the tuning voltage below that required for the 'worst case' combination of component tolerances in the tuner and other tuning system components. This ensures that once the default values have been stored the appropriate channel (as shown above) can always be found by tuning 'up' the band rather than 'down' the band.

12. ADJUSTMENTS.

HT supply (109.5V/115V)
Reduce the A1 brightness and contrast to a minimum, adjust RV806 for 109.5V across CE814 for televisions with FST tubes (15"/36cm and 21"/51cm), and 115V for standard tubes (14"/34cm and 20"/48cm).

A.G.C.
Correctly tune the receiver to a 10mV R.F. modulated carrier at approximately channel E 58 (767.25MHz). Monitor the tuner output (pin 9 PL101) with an oscilloscope and probe calibrated to read accurately at 40MHz. Adjust RV101 to obtain the following level at the peak to peak sync excursions:-

UK models 1.2V
German models 325mV
Other models 600mV

A.F.C., System I.
Adjust L103 to give 2.5V at pin 12, PL101 when 39.5MHz is injected into the SAW filter.

Vision Tank, System I.
Adjust L104 to display a square corner without overshoot, or excessive 'rounding', at the beginning of the peak white section of a colour bars signal at the emitter of TR101.

A.F.C., System B,G,D,K.
Adjust L107 to give 2.5V d.c., pin 3, PL101 when 38.9MHz is injected into the SAW filter.

Vision Tank, System B,G,D,K.
Adjust L106 to display a square corner without overshoot, or excessive 'rounding', at the beginning of the peak white section of a colour bars signal at the emitter of TR101.

Sound Tank, System B,G,D,K.
Adjust L105 until a null point is found where the video information at pin 21, IC101, is at minimum.

Sound Coil 5.5MHz., System B,G,D,K.
Adjust L103 for minimum distortion at pin 11, IC101, when the receiver is fed with a signal containing a 5.5MHz sound carrier frequency modulated with 1kHz.

Sound Coil 6.5MHz., System B,G,D,K.
Adjust L104 for minimum distortion at pin 11, IC101, when the receiver is fed with a signal containing a 6.5MHz sound carrier frequency modulated with 1kHz.

* Secam Ident Coil.
Adjust L502 for maximum voltage at pin 23, IC543.

* Bell Filter.
Adjust L503 for minimum overshoot on R-Y and B-Y signals at pins 60 and 62 of IC543.

* R-Y and B-Y Demodulators.
Adjust L510 and L511for equal levels during blanking and black parts of signal at pins 1 and 63 of IC543. See waveform diagrams.

Timebase.
Width - Adjust L402 (Line width) and RV535 (Line phase) for correct picture width and centring.
Height - Adjust RV547 (Field height) and RV312 (Field shift) for correct screen height and centring.

Luma Drive.
Adjust RV505 to give 400mV black to white level at pin 58, IC543.

Delay Line Amp.
Adjust RV560 to minimize Hanover bars with signal containing unswitched chroma.

Delay Line Phase.
Adjust L508 to minimize Hanover bars.

R.G.B. Background A1 & Focus.
The picture tube-base panel includes the supplies to the tube electrodes with their associated components for circuit protection. Internal spark gaps are fitted in the tube socket for connection to the tube external dag coating. Also included on the panel are the video amplifiers TR201,TR202, and TR203, and their preset adjustments. The focus and A1 supplies are embodied in the diode-split transformer (T402).

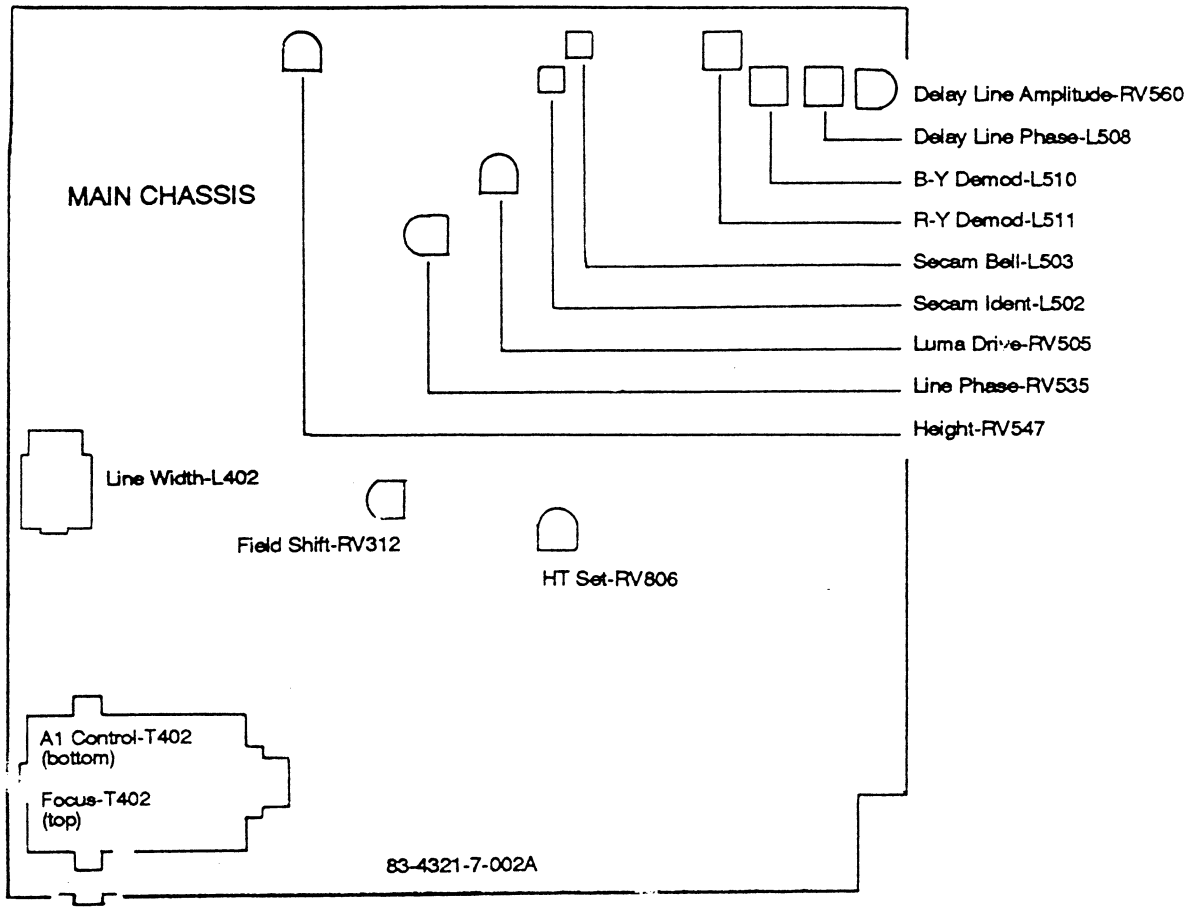
To adjust the red, green and blue backgrounds; reduce the A1 control to minimum. Adjust the user brightness and contrast controls to their normalized settings and set the colour saturation control to minimum.
Adjust each of the background controls R202,R203 and R204 so that the black level measured at each tube cathode (R904, R905, and R906) is 150V.

A1 Control.
Adjust the A1 control (lower adjustment on T402) for correct overall black level on the display. Grey-scale corrections may now be carried out with only two of the background preset controls.

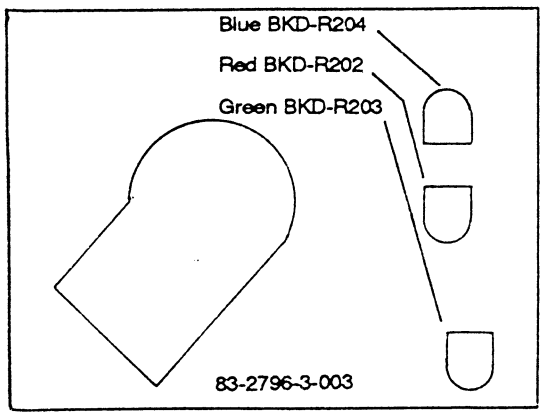
Focus.
Adjust the upper control on T402 for optimum focus in the centre of the screen.

* For these adjustments the CTV must be receiving Secam transmissions.

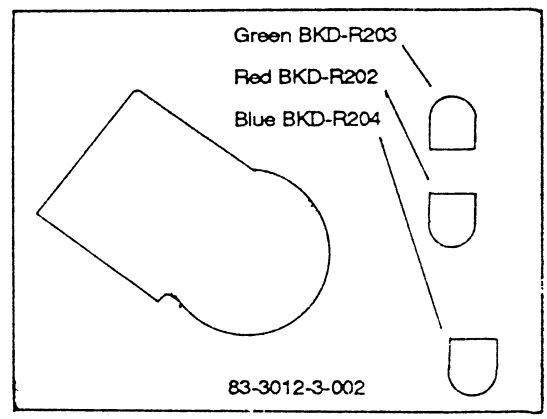
12.1 Adjustment Locations



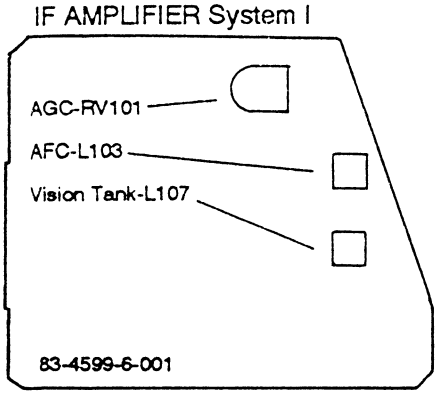
STD NECK TUBE BASE



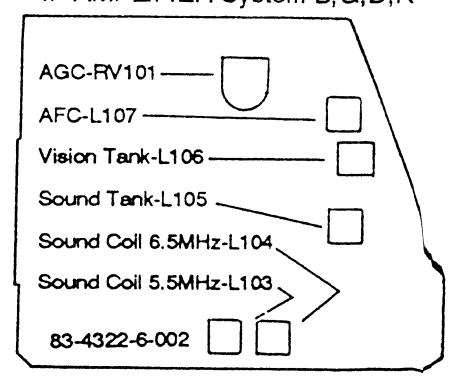
MINI NECK TUBE BASE

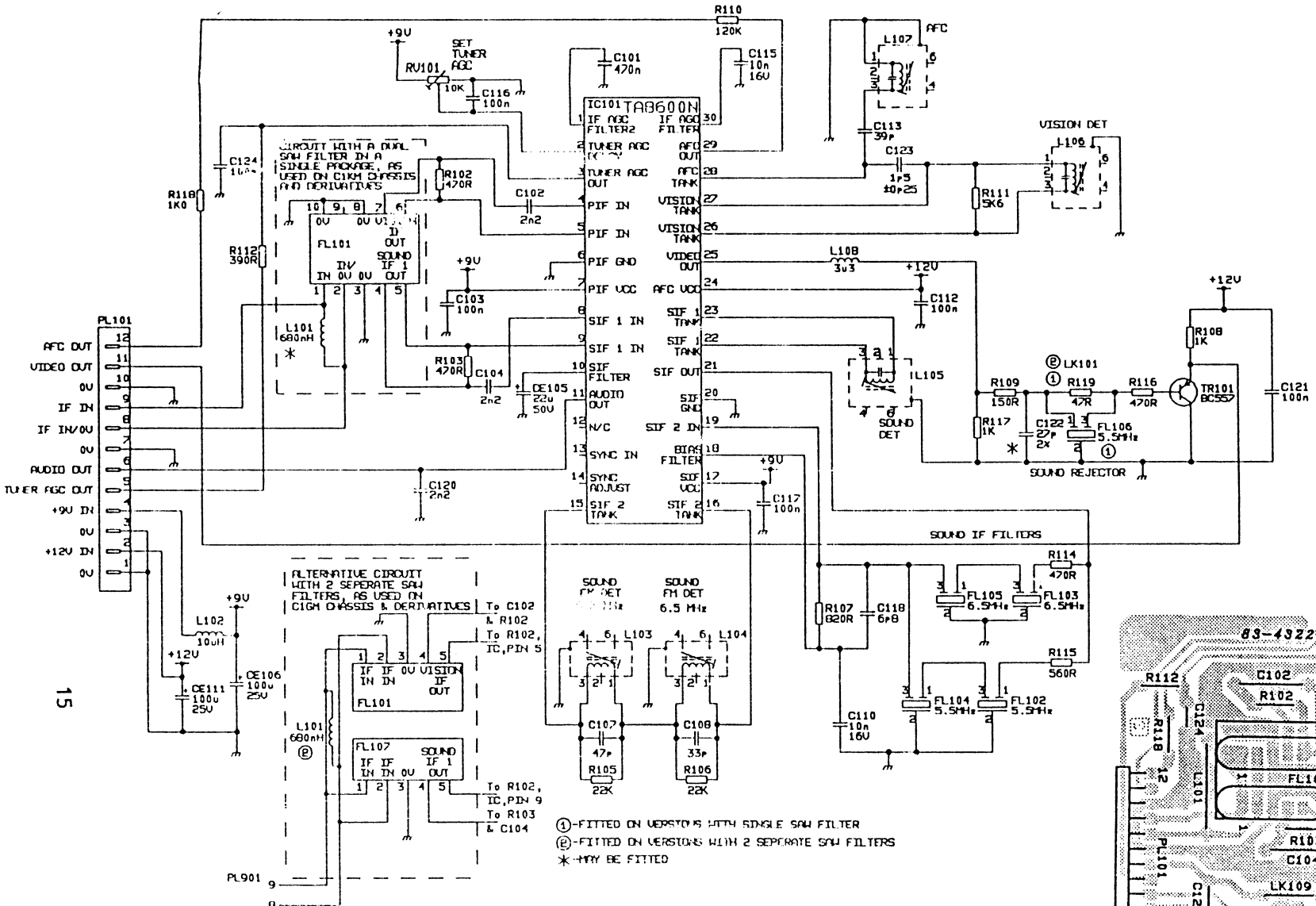


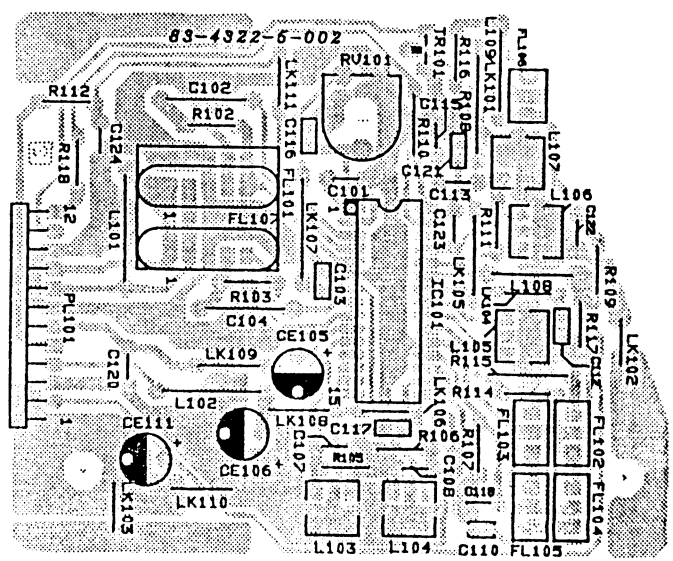
IF AMPLIFIER System I



IF AMPLIFIER System B,G,D,K

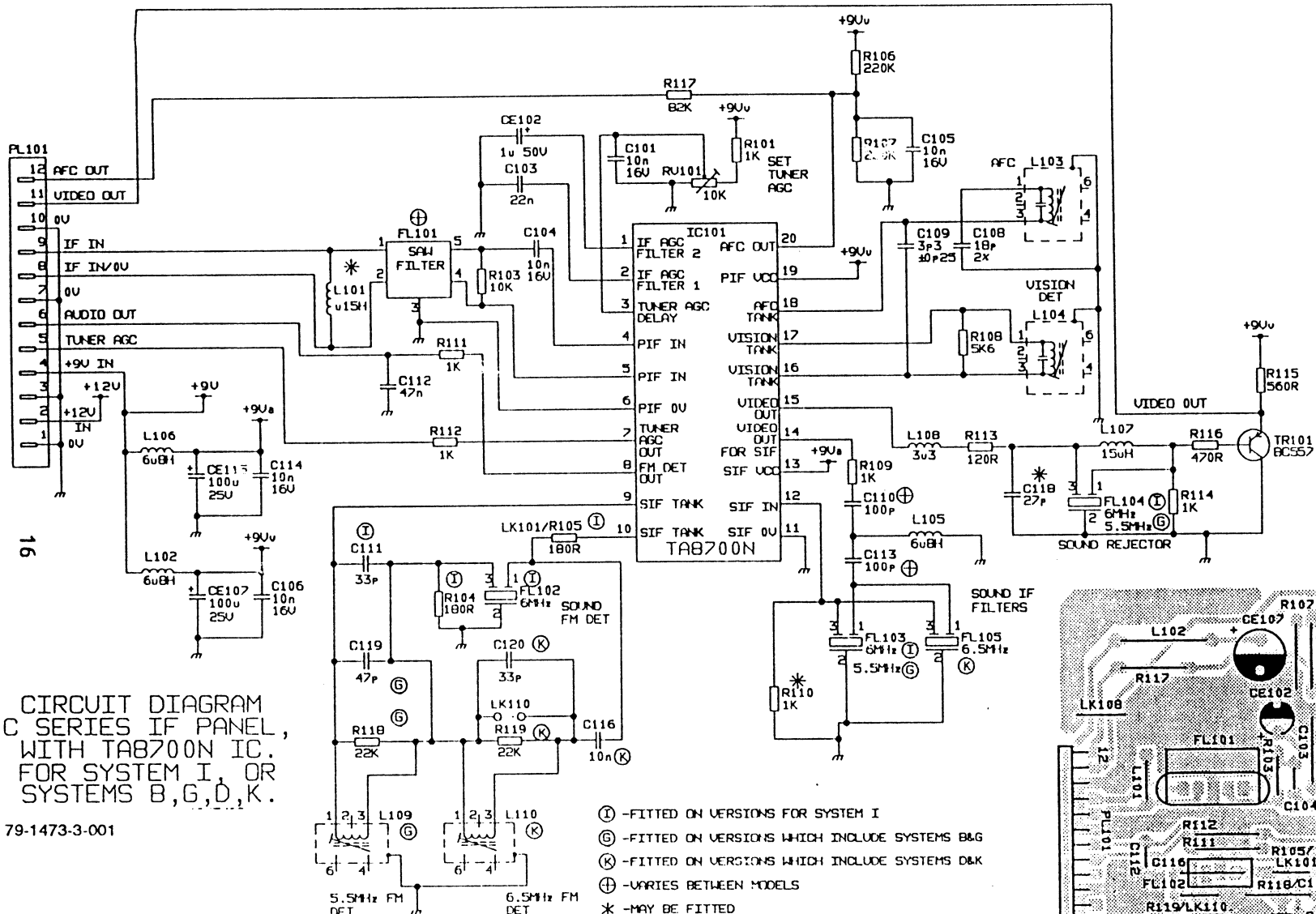






CIRCUIT DIAGRAM
'C' SERIES IF PANEL
WITH TA8600N IC:-
QUASI-PARALLEL SOUND VERSIONS
FOR SYSTEMS B,G,D,K.

79-146[illegible]3-001



CIRCUIT DIAGRAM
C SERIES IF PANEL,
WITH TA8700N IC.
FOR SYSTEM I, OR
SYSTEMS B,G,D,K.

79-1473-3-001

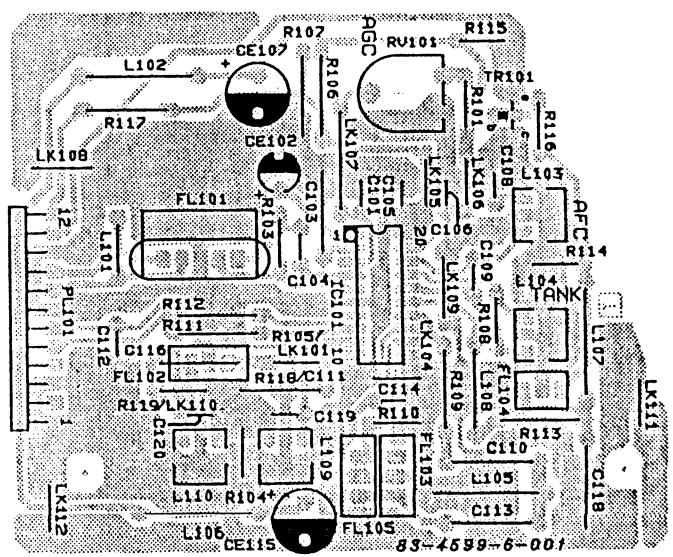
Ⓘ -FITTED ON VERSIONS FOR SYSTEM I

Ⓖ -FITTED ON VERSIONS WHICH INCLUDE SYSTEMS B&G

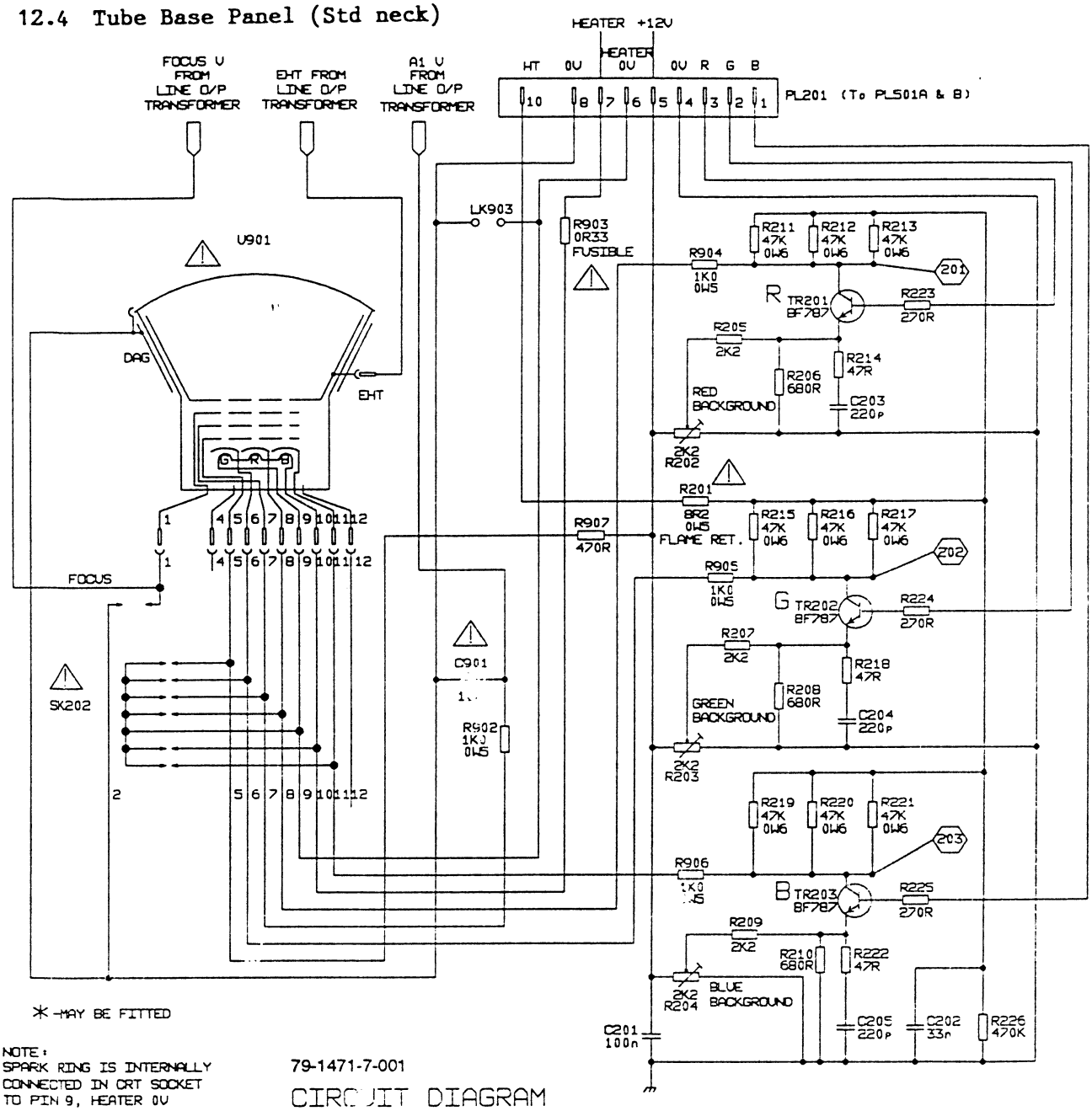
Ⓚ -FITTED ON VERSIONS WHICH INCLUDE SYSTEMS D&K

⊕ -VARIES BETWEEN MODELS

✳ -MAY BE FITTED



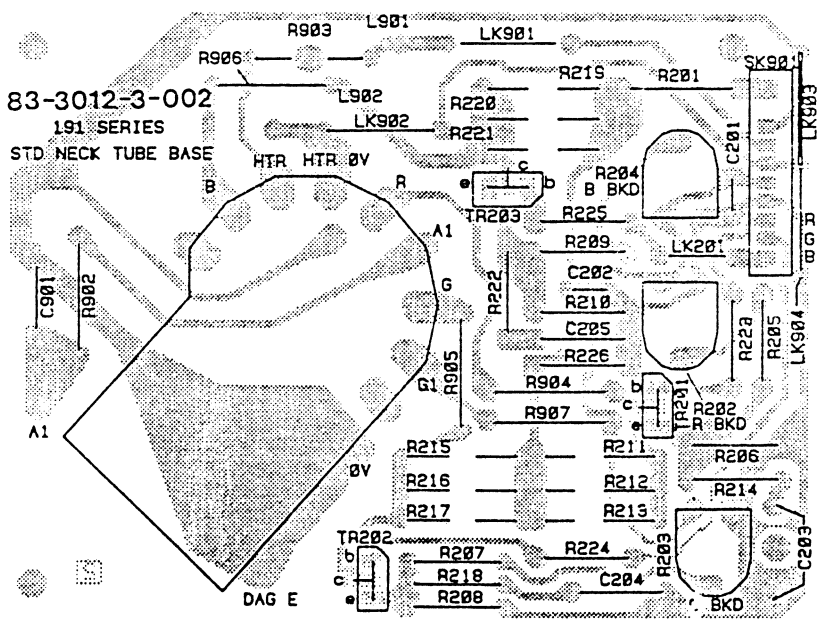
12.4 Tube Base Panel (Std neck)

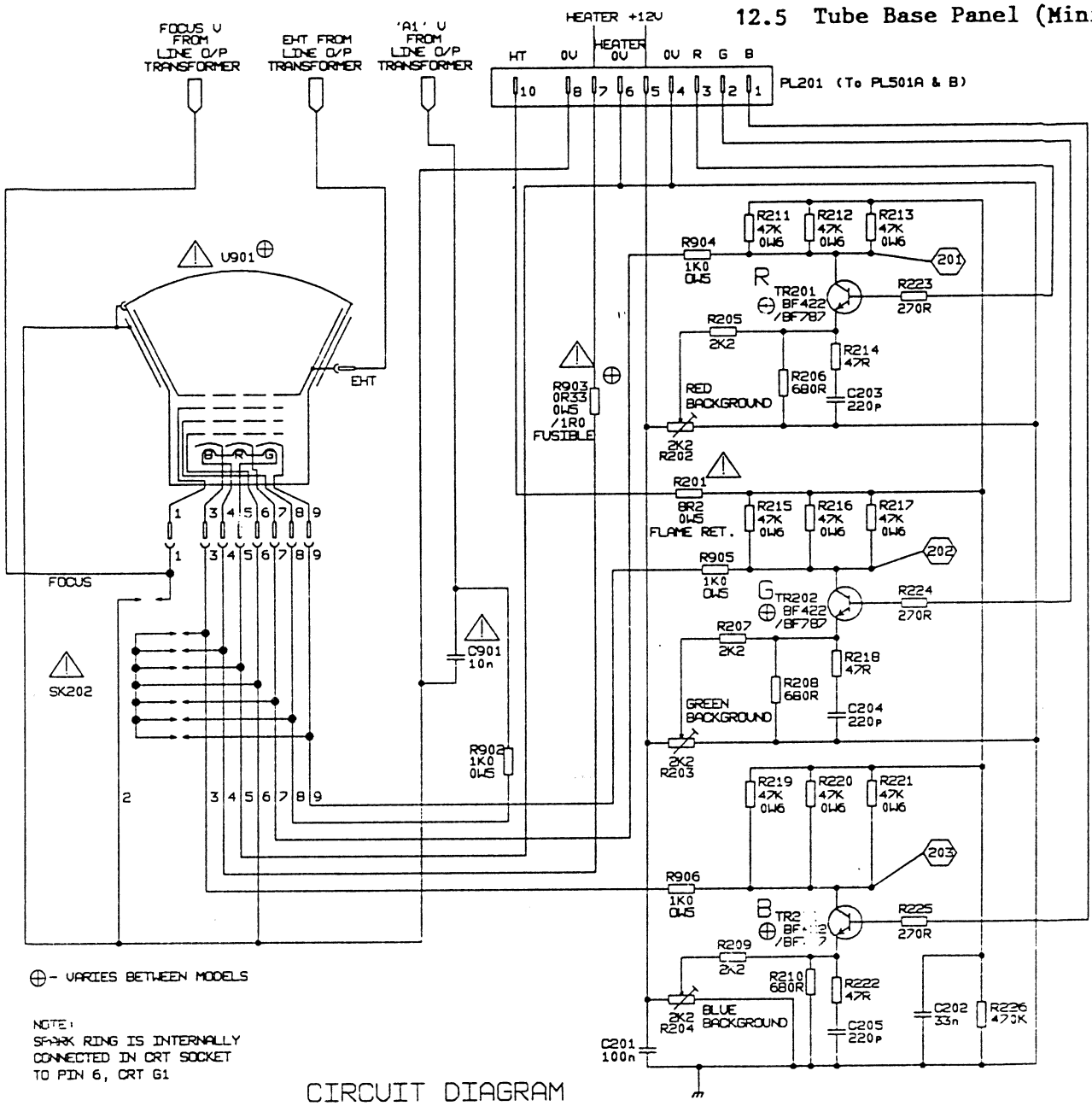


NOTE:
SPARK RING IS INTERNALLY CONNECTED IN CRT SOCKET TO PIN 9, HEATER 0V

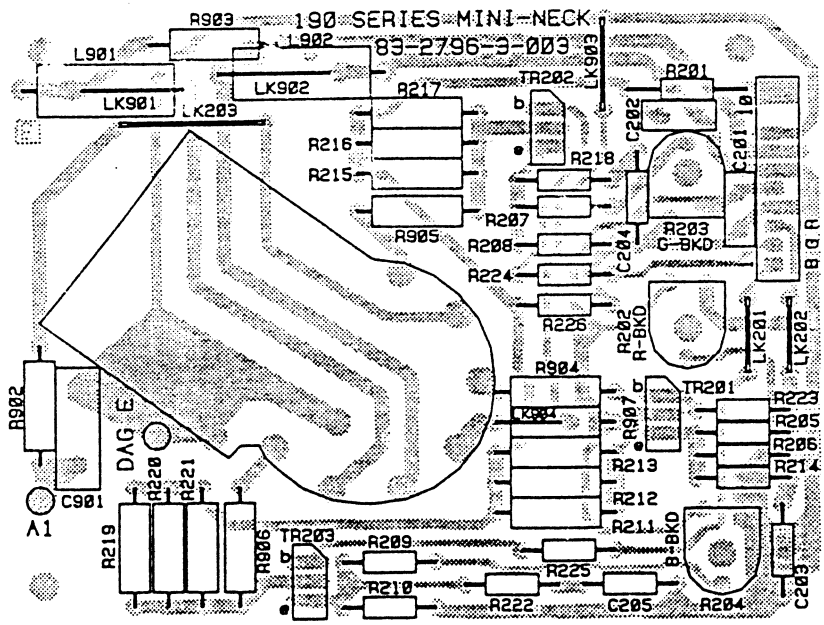
79-1471-7-001

CIRCUIT DIAGRAM
C SERIES TUBE BASE PANEL
STANDARD NECK CRT (29.5mm)

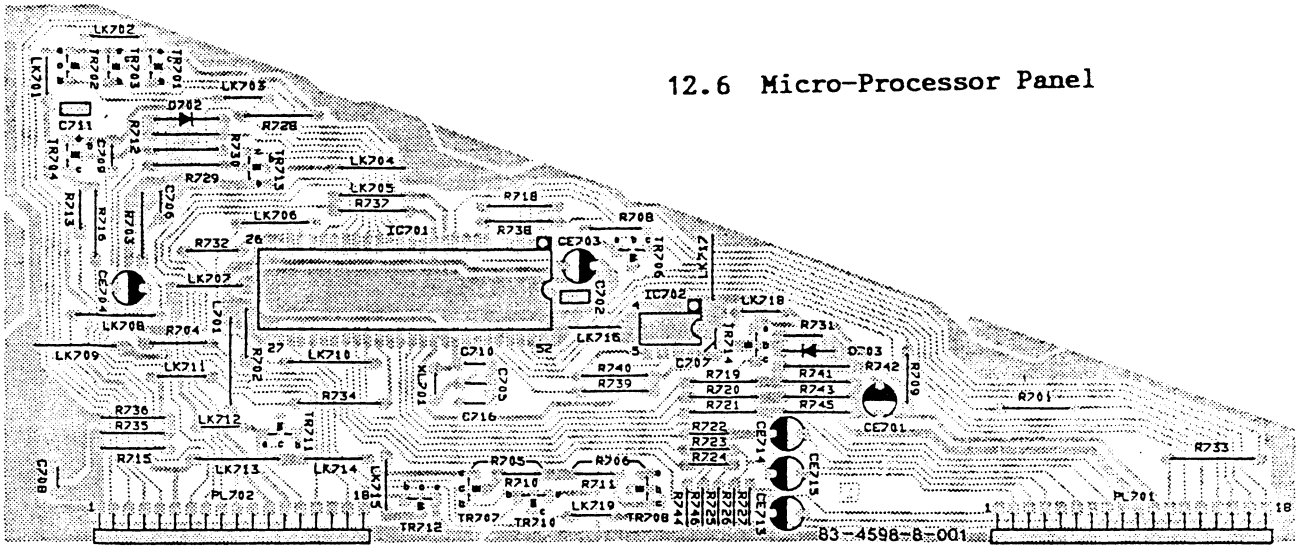


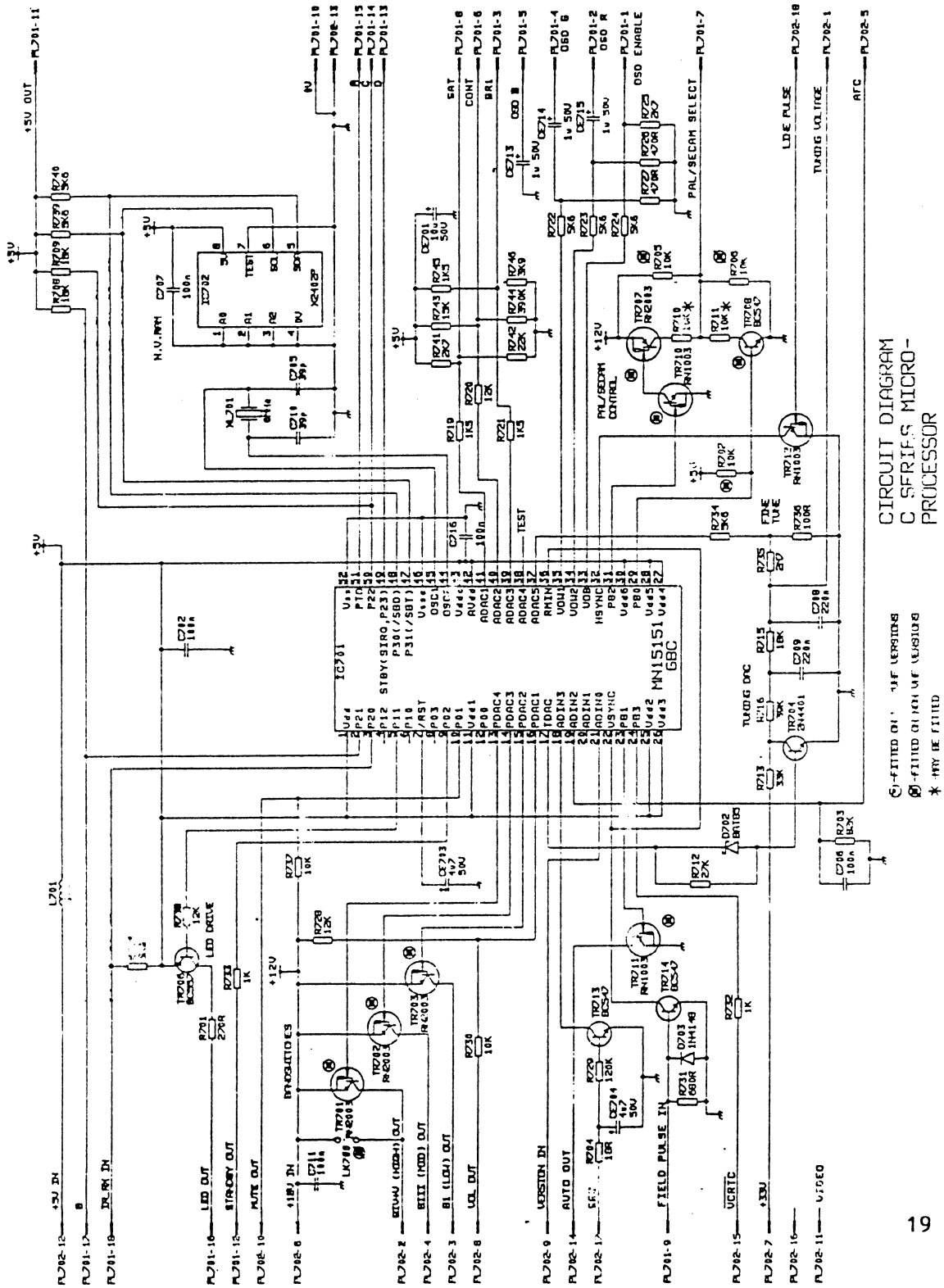


CIRCUIT DIAGRAM
C SERIES TUBE BASE PANEL
MINI NECK CRT (22.5mm)
79-1470-9-001

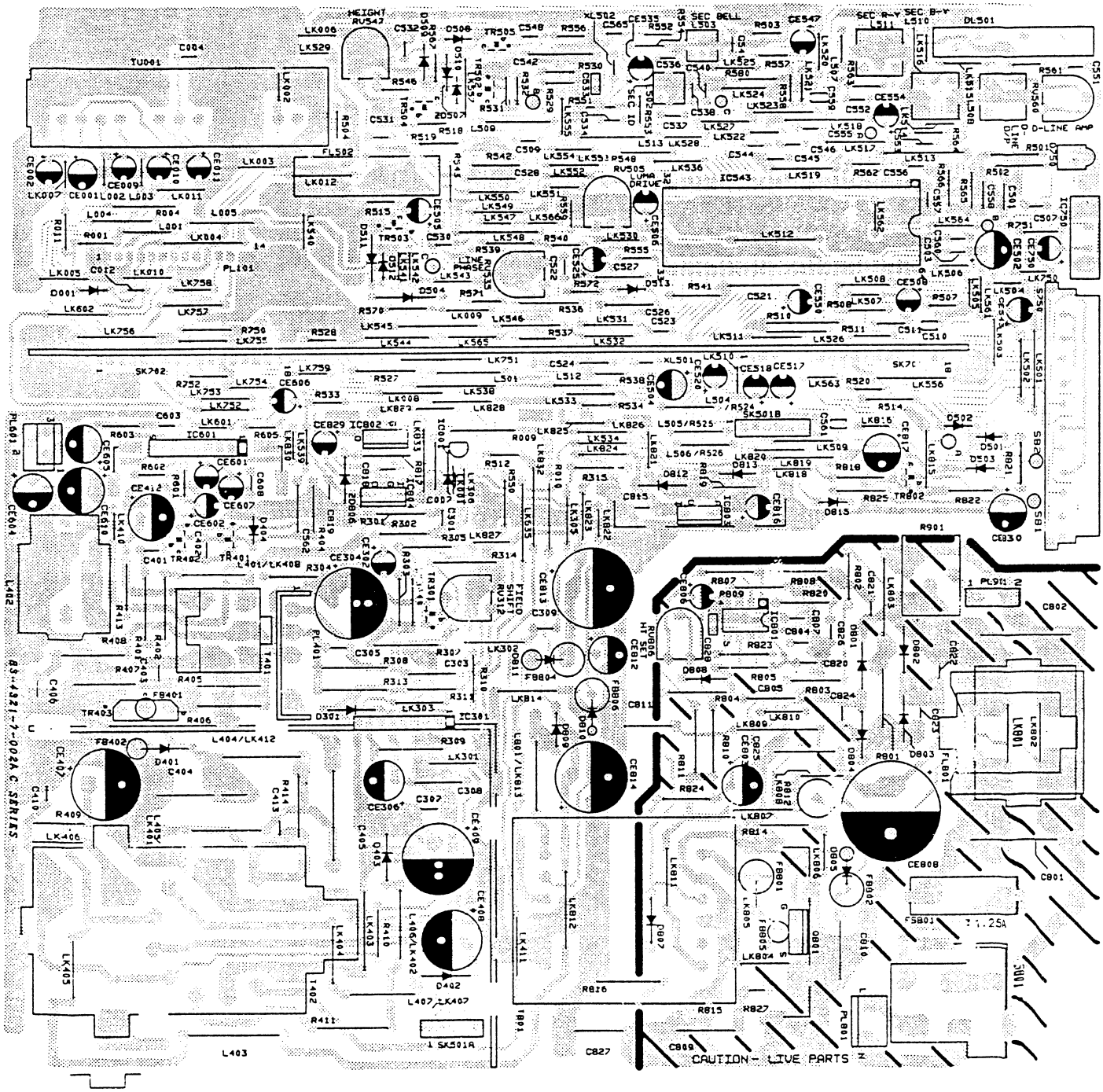


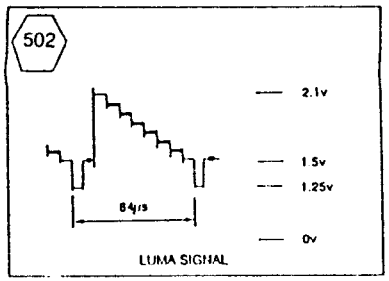
12.6 Micro-Processor Panel

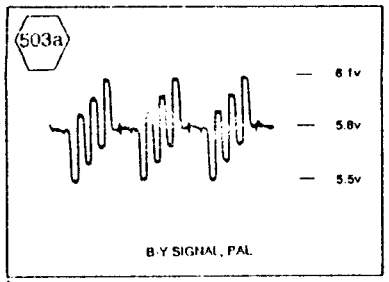


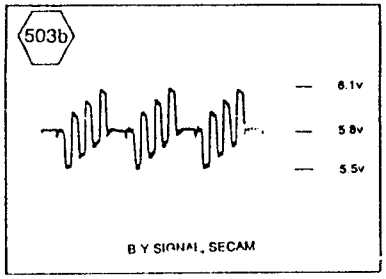


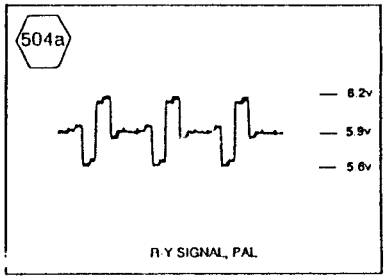
15. C SERIES MAIN CHASSIS COMPONENT LAYOUT

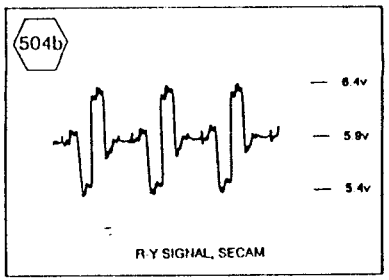


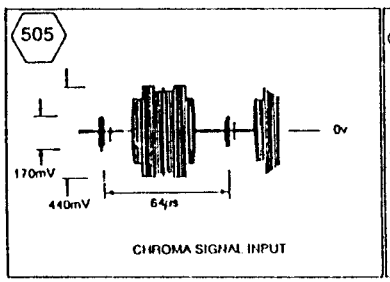

502
2.1v
1.5v
1.25v
0v
64µs
LUMA SIGNAL

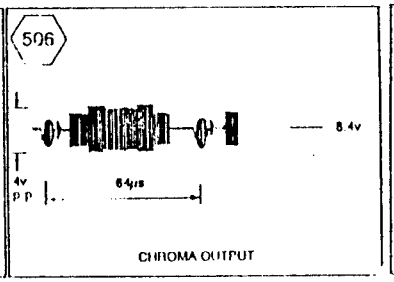

503a
6.1v
5.8v
5.5v
B-Y SIGNAL, PAL

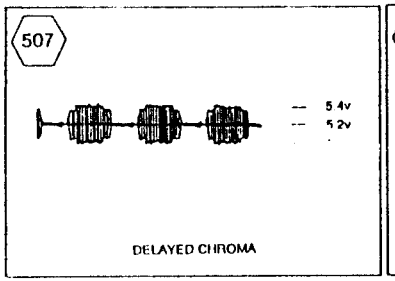

503b
6.1v
5.8v
5.5v
B-Y SIGNAL, SECAM

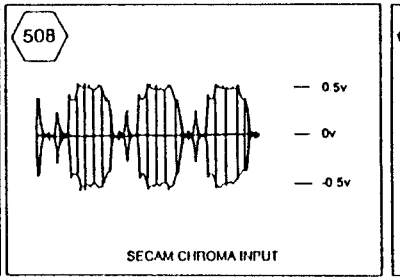

504a
6.2v
5.9v
5.6v
R-Y SIGNAL, PAL

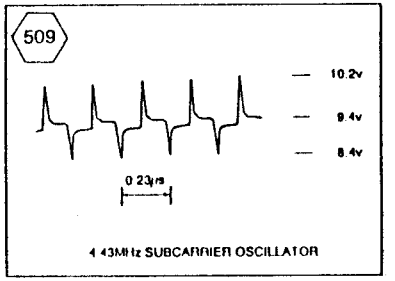

504b
6.4v
5.9v
5.4v
R-Y SIGNAL, SECAM

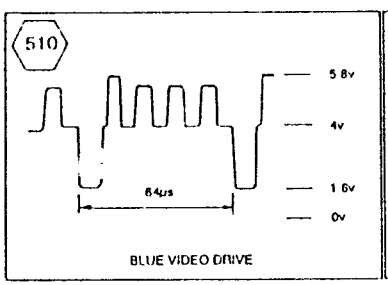

505
0v
170mV
440mV
64µs
CHROMA SIGNAL INPUT

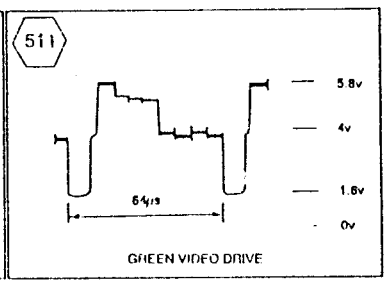

506
8.4v
4v
p-p
64µs
CHROMA OUTPUT

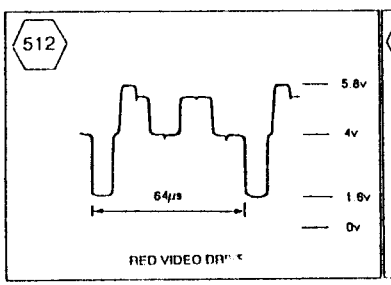

507
5.4v
5.2v
DELAYED CHROMA

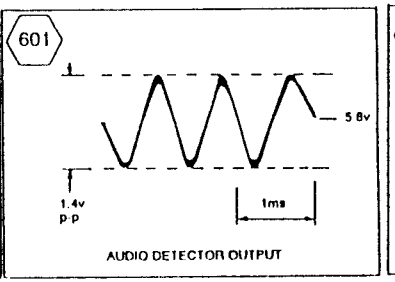

508
0.5v
0v
-0.5v
SECAM CHROMA INPUT

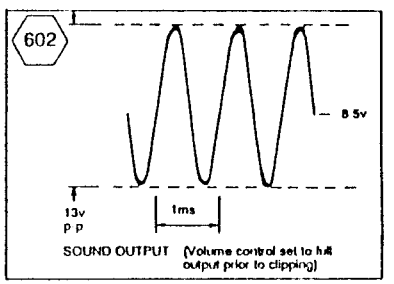

509
10.2v
9.4v
8.4v
0.23µs
4.43MHz SUBCARRIER OSCILLATOR

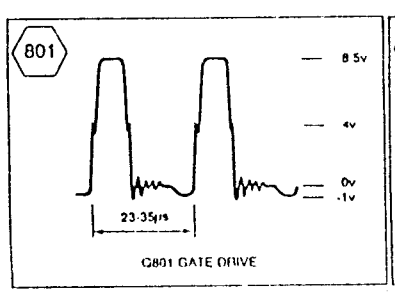

510
5.8v
4v
1.6v
0v
64µs
BLUE VIDEO DRIVE

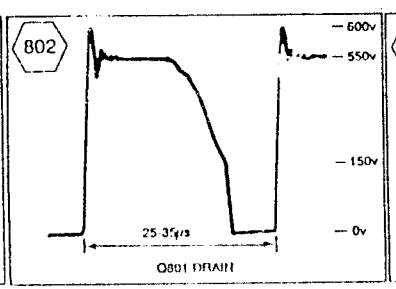

511
5.8v
4v
1.6v
0v
64µs
GREEN VIDEO DRIVE

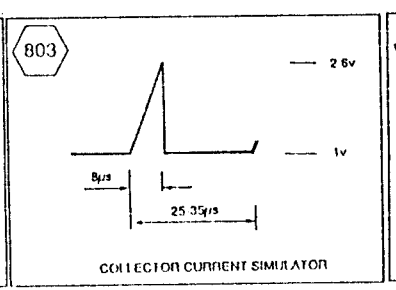

512
5.8v
4v
1.6v
0v
64µs
RED VIDEO DRIVE

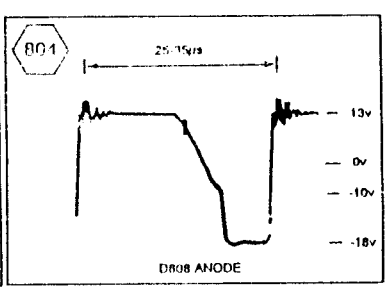

601
5.8v
1.4v
p-p
1ms
AUDIO DETECTOR OUTPUT


602
8.5v
13v
p-p
1ms
SOUND OUTPUT (Volume control set to full output prior to clipping)

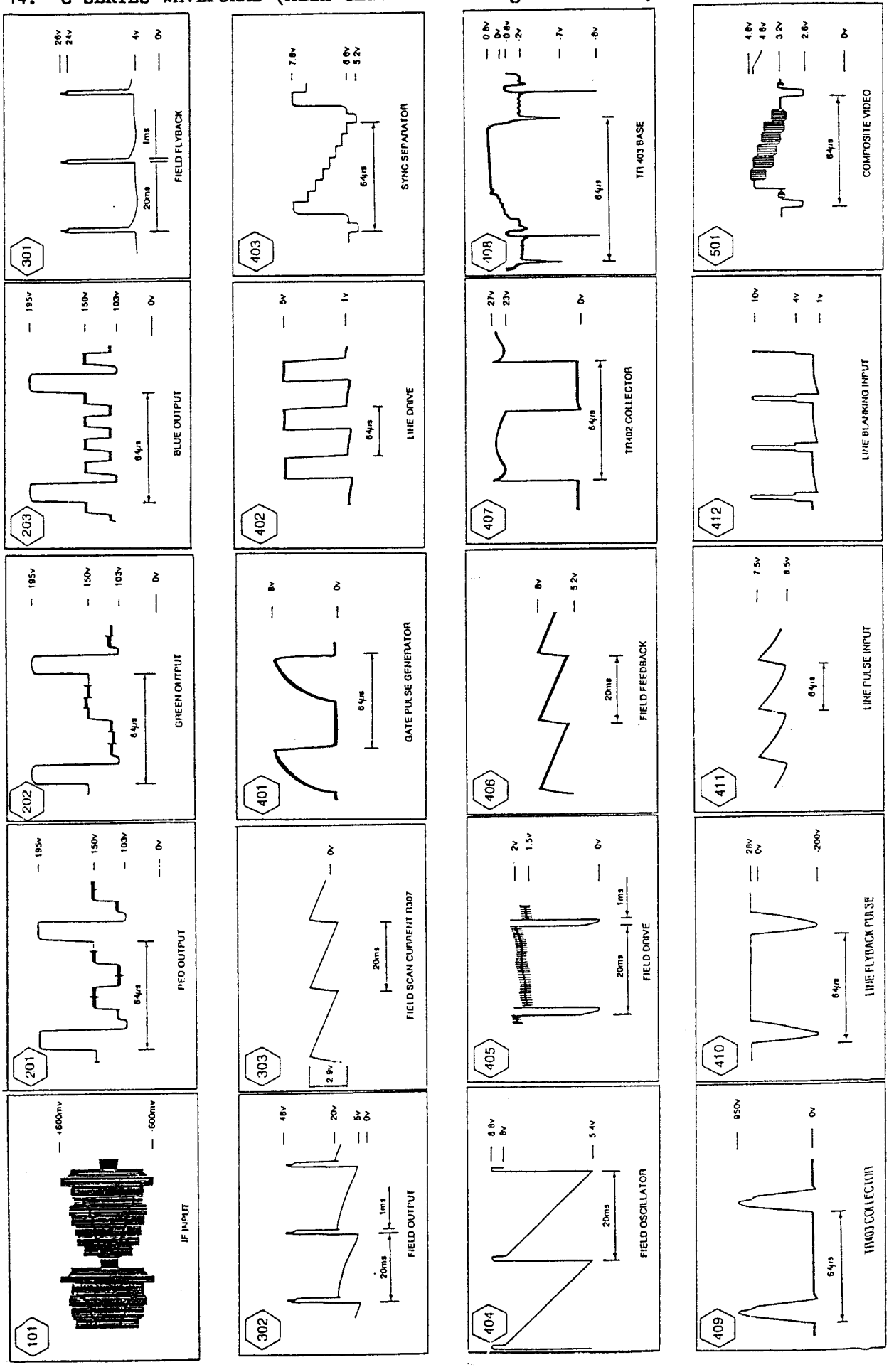

801
8.5v
4v
0v
-1v
23.35µs
Q801 GATE DRIVE


802
600v
550v
150v
0v
25.35µs
Q801 DRAIN


803
2.6v
1v
8µs
25.35µs
COLLECTOR CURRENT SIMULATOR


804
13v
0v
-10v
-18v
D808 ANODE

14. C SERIES WAVEFORMS (Main Chassis and Plug-in Modules)



TUNER

AUDIO AMP
IC601
AN5265

FIELD OUTPUT AMP
IC301
TDA3653B

TO IF PANEL

TO LOUDSPEAKER

LUMA PROCESSING

SECAM CHROMA REJECTOR SWITCH

WIRING HARNESS TO TUBE BASE

VCR TC SWITCH

LINE SYNC PROCESSING

FIELD RAMP GENERATOR

FIELD OUTPUT SUPPLY

VIDEO OUTPUT H.T. SUPPLY

LINE OUTPUT TRANSFORMER

LINE OUTPUT

LINE DRIVE

TO HORIZONTAL DEFLECTION COILS

TO VERTICAL DEFLECTION COILS

LINEWIDTH COIL

IC543
TA8659CN

COLOUR DECODER

DELAY LINE

SECAM BELL FILTER

SECAM IDENT

PAL SUBCARRIER OSC

LOCAL CONTROLS

POWER SUPPLY

12V REGULATOR

9V REGULATOR

5V REGULATOR

SK701 & SK702 CONNECT TO MICROPROCESSOR PANEL

TO DEGAUSS COIL

MAINS ISOLATION BARRIER

- -FITTED ON SECAM VERSIONS
- -FITTED ON UHF/VHF VERSIONS
- -FITTED ON NON VHF VERSIONS
- -VARIES BETWEEN MODELS
- -CRITICAL SAFETY COMPONENT
- -MAY BE FITTED
- -HAVE STUFFA MONITORING POINT

CIRCUIT DIAGRAM
C SERIES MAIN PANEL
79-1474-1-001